Aprobat pentru anul universitar 2010/2011

FIŞA DISCIPLINEI

Denumirea disciplinei :		Research Methods in Advanced Computing Architectures			
Codul disciplinei:					
Programul de studii:		ADVANCED COMPUTING SYSTEMS (MSc Program, in English)			
Catedra:		Calculatoare si automatizari			
Facultatea:		Inginerie			
Universitatea:		"Lucian Blaga" din Sibiu			
Anul de studiu**:**	1	Semestrul	1	Tipul de evaluare finală	**E**
Regimul disciplinei (DI=obligatorie/ DO=opţională/DF=liber aleasă):			**DI**	Numărul de credite:	**10**
Categoria formativă a disciplinei (DF=fundamentală.; DI=inginereşti; DS=specialitate; DC=complementară)					**DS**
Total ore din planul de învăţământ				Total ore pe semestru:	70
Titularul disciplinei: Prof. univ. dr. ing. Lucian VINTAN, m.c. ASTR					

Numărul total de ore (pe semestru) din planul de învăţământ					
Total ore/ semestru	**C**	**S**	**L**	**P**	**Total**
	3		**2**		**5**

Obiective:	• Understanding what is research in Advanced Computer Architecture (Modelling, Trace_Driven & Execution_Driven Simulation, Benchmarking, Iterative Optimization, Automatic Design Space Exploration, Writing Papers, etc.) • Understanding some research papers, technical reports, PhD Theses, etc. in Advanced Computing Architectures domain. Understanding the multicore and manycore research paradigm. • Developing a research project and writing a scientific paper based on it
Competenţe specifice disciplinei	**1. Cunoaştere şi înţelegere:** • Intelegerea unor arhitecturi novatoare, avansate, de procesare a informatiei precum si a metodologiilor de cercetare ale acestora • O viziune unificata, holistica, asupra ingineriei calculatoarelor
	2. Explicare şi interpretare: • Explicarea si interpretarea calitativa a rezultatelor cantitative obtinute prin simulari complexe. Intelegerea actiunii diversilor parametri asupra performantei sistemelor avansate de calcul. Stapanirea complexitatii proiectelor arhitecturale. • Intelegerea aprofundata a dependentei dintre performanta aplicatiilor software si caracteristicile arhitecturii hardware

3. Instrumental – aplicative • Dezvoltarea aptitudinilor practice de lucru cu sisteme de calcul avansate, simulatoare complexe si medii de dezvoltare, compilatoare, debuggere, benchmark-uri etc., aferente unor microarhitecturi de calcul moderne, in vederea proiectarii-dezvoltarii de aplicatii hardware-software integrate si evaluarii performantelor acestora
4. Atitudinale: • capacitatea de utilizare a mijloacelor moderne de documentare şi de simulare/evaluare a arhitecturilor complexe; • crearea unui limbaj tehnic adecvat analizelor si dezvoltarilor experimentale in domeniul microprocesoarelor si multiprocesoarelor; • capacitatea studentilor de a lucra in echipe de cate 2-4 membri, in vederea efectuarii unor aplicatii relative complexe.

Scientific Contents

Topic's Curricula - http://webspace.ulbsibiu.ro/lucian.vintan/index.html#11

1. Introduction to prediction and speculative execution implemented in Computer Architectures	3 hours
2. Advanced Branch Prediction Methods 2.1 Dynamic Neural Branch Prediction. Genesis 2.1.1 Previous Work in the Field 2.1.2 First Neural Dynamic Branch Prediction Models 2.2 Trace Driven Simulation Results 2.3 A Static Branch Neural Predictor 2.4 Some Comments to Neural Branch Prediction Idea 2.5 Making it feasible: Perceptron Branch Predictors **2.6 Towards cross-fertilization between computer architecture and other computer science fields** 2.6.1 Some oher Neural Approaches in Computer Arhitecture 2.6.2 A Markovian Branch Predictor 2.6.3 Genetic Branch Predictors	3 hours
3. Understanding Some Present-Day Branch Prediction Limits 3.1 Unbiased Branches Problem and Related Works 3.2 Finding Unbiased Branches. Research Methodology 3.3 Some Experimental Results (Simulation) 3.4 Some Conclusions and Further Work	3 hours
4. Pre-Computing Branches (PCB) 4.1 Introduction 4.2 The Pre-Computed Branch Algorithm 4.3 Complexity and Costs Evaluations 4.4 Performance Evaluations through Simulation 4.5 Some Conclusions and Further Work 4.6 Appendix. PCB Algorithm	3 hours
5. Dynamic Instruction Reuse 5.1 Fetch Bottleneck. Dynamic instruction reuse through trace-cache processors 5.2 Issue (Data- Flow) Bottleneck. Dynamic Instruction Reuse. Function Reuse	3 hours
6. Dynamic Instruction Value Prediction and Speculation 6.1 Introduction to Value Prediction 6.2 Predicting Load Instructions 6.3 Generalised Value Prediction	3 hours

6.3.1 Computational Predictors 6.3.2 Contextual Predictors 6.3.3 Hybrid predictors 6.4 The Value Prediction Speedup. A Simple Analytical Model	
7. Focalizing Dynamic Value Prediction to CPU's Registers ***7.1 The Register Value Predictor Concept*** 7.2 Register Value Predictors 7.3 Simulation Methodology and Experimental Results 7.4 Register Value Prediction using Meta-predictors 7.5 Meta-predictors' Simulations and Quantitative Evaluations 7.6 Conclusions and some Further Work Ideas	3 hours
8. Neural Networks Models with Applications in Ubiquitous Computing. Next Location Prediction 8.1 Introduction to *UbiCom* 8.2 A Related Concept: Autonomic Computing 8.3 The Next Location Prediction Problem in an *UbiCom* Environment ***8.4 Person Movement Prediction Using Neural Networks*** 8.5 Experimental Results. Analysis and Comments 8.6 Some Conclusions and Further Work Ideas	3 hours
9. Hidden Markov Models with Applications in Ubiquitous Systems. Next Location Prediction 9.1 Applications based on Hidden Markov Models 9.2 Discrete Markov Processes **9.3 Hidden Markov Models of order 1** **9.4 Prediction algorithm using a HMM of order 1** ***9.5 A possible generalization: Hidden Markov Models of order R>1*** **9.6 Prediction algorithm using a HMM of order R>1** 9.7 Methodology and Experimental Results **9.8 Some Conclusions**	6 hours
10. Multiprocessor systems on chips (MPSOCS). Why MPSOCS? Challenges, design methodologies, hardware architectures, software, Performance modeling and analysis. Design of communication architectures for MPSOCS. Memory systems and compiler support for MPSOCS. Component-based design. Models of computation for MPSOCS. Multicores based on speculative-execution processors. Automatic Design Space Exploration (heuristic algorithms, complex tool implementation). Networks on a Chip simulator and optimal tasks mapping for a parallel software application	12 hours
TOTAL	**42 hours**

II. Applications' Curricula

Each student will chose and develop a research project belonging to the following proposals:

- Next Location (Context) Prediction in an intelligent *UbiCom* ambient (Augsburg benchmarks belonging to the Smart_Doorplates project - we have the benchmarks through an institutional collaboration; Nokia benchmarks – free on Nokia's site, etc.) A Neural Approach. A Markov Approach. A Hidden Markov Models Approach.

- Integrating Dynamic Instruction Reuse (DIR) in an advanced superscalar/SMT microarchitecture (*Kilo-Instruction Processor* – developed at UPC Barcelona; we have the simulator through an institutional collaboration with DAC UPC. Simulations on SPEC 2000 benchmarks)

- Integrating Dynamic Value Prediction (DVP) in an advanced superscalar/SMT microarchitecture (*Kilo-Instruction Processor* – developed at UPC Barcelona; we have the simulator through an institutional collaboration. Simulations on SPEC 2000 benchmarks)

- Focalising Dynamic Value Prediction to CPU's Context. Simulations on SPEC 2000 benchmarks

- Developing an Adaptive Meta-Predictor for a Hybrid Dynamic Value Predictor (multiple DVPs). Simulations on SPEC 2000 benchmarks

- Integrating Advanced Hybrid Branch Predictors (Two Level Adaptive + Neural, Perceptron) in an advanced superscalar microarchitecture. Simulations on SPEC 2000 and INTEL CBP benchmarks

- Understanding and Predicting Indirect Branch Behavior. Simulations on SPEC 2000 benchmarks and some developed specific C/C++ programs.

- Detecting and Predicting Unbiased Branches in *Kilo-Instruction Processor* Architecture. Simulations on SPEC 2000 and INTEL CBP benchmarks

- Solving Fetch Bottleneck. Trace-Processor Simulation (SPEC 2000)

- Investigating Procedural/Object Programming Corpus' Influence on DIR/DVP

- Simulating Multicore Architectures. Full system simulation

- Automatic Design Space Exploration in Multicore Systems

- Networks on a Chip simulator and optimal tasks mapping for a parallel software application

- Parallel Programming on IBM Cell BE architecture (accelerating some Computational Fluid Dynamics Programs)

Finally, each student will present an technical report (TR) & PPT presentation and a simulator concerning this research project. Based on the TR it will be developed a scientific paper.

REFERENCES (selective):

1. VINTAN N. LUCIAN – *Arhitecturi de procesoare cu paralelism la nivelul instructiunilor*, Editura Academiei Romane, Bucuresti, 2000 (264 pg.), ISBN 973-27-0734-8 – comanda la **www.ear.ro**, Bibl. ULBS, cota 45.351 (15 ex. la Biblioteca ULBS)
2. VINTAN LUCIAN, FLOREA ADRIAN - *Sisteme cu microprocesoare - aplicatii*, Editura Universitatii "L. Blaga" din Sibiu, ISBN 973-9410-46-4 , Sibiu, 1999 (245 pg.) Bibl. Univ. Sibiu, cota 43.800 (15 ex. intern + 15 ex. schimb interbibliotecar)
3. VINTAN N. LUCIAN, FLOREA ADRIAN – *Microarhitecturi de procesare a informatiei*, Editura Tehnica, Bucuresti, ISBN 973-31-1551-7, cota bibl. ULBS 45.797 (16 schimb+14 intern bibl.ULBS), 2000 (312 pg)
4.FLOREA ADRIAN, VINTAN N. LUCIAN – *Simularea si optimizarea arhitecturilor de calcul in aplicatii practice*, Editura Matrix Rom, Bucuresti, ISBN 973-685-605-4, 2003 (443 pg. + CD atasat), Bibl. Univ. Sibiu - cota 48.351 (4 ex. la Biblioteca ULBS + 4 ex. schimb interbibliotecar); comenzi la **www.matrixrom.ro**
5. VINTAN LUCIAN.- *Generaţia următoare,* în revista PC-Report, nr.3, Editura Computer Press Agora, ISSN 1220-9856, martie, 2000
6.VINTAN LUCIAN.- *Procesorul IA-64: între evoluţie şi revoluţie,* în revista PC-Report, nr.5, Editura Computer Press Agora, ISSN 1220-9856, mai, 2000
7.VINTAN LUCIAN.- *Organizarea si proiectarea microarhitecturilor. Note de curs* (pdf, 270 pagini A4), URL: **http://webspace.ulbsibiu.ro/lucian.vintan**
7. HENNESSY J., PATTERSON D. - *Computer Architecture: A Quantitative Approach*, Morgan Kaufmann (Elsevier), 3rd Edition, 2003
8. PATTERSON D., HENNESSY J. - *Computer Organization and Design, The Hardware/ Software Interface*, Morgan Kaufmann Publishers, 2nd Edition, 1998 (traducere romaneasca la Editura ALL, Bucuresti, 2000)
9. FISHER J., FARABOSCHI P., YOUNG C. – *Embedded Computing***,** Morgan Kaufmann Publishers (Elsevier), 2005
10. HAYES J. – *Computer Architecture and Organization*, Third Edition, McGraw Hill, 1998
11. JERRAYA A., WOLF W. (Editors) – *Multiprocessors Systems on Chips*, Morgan Kaufmann Publishers (Elsevier), 2005
12. VINTAN N. LUCIAN – *Prediction Techniques in Advanced Computing Architectures* (in English Language), Matrix Rom Publishing House, Bucharest, 2007 (292 pg.); comenzi la **www.matrixrom.ro**
13. VINTAN N. LUCIAN – *Documentatii (articole, prezentari PPT, teze etc.) aferente acestei discipline,* URL: **http://webspace.ulbsibiu.ro/lucian.vintan/index.html#11**
14. L. N. VINŢAN - *Direcţii de cercetare în domeniul sistemelor multicore / Main Challenges in Multicore Architecture Research*, Revista Romana de Informatica si Automatica, ISSN: 1220-1758, ICI Bucuresti, 2009
15. VINTAN L. N., FLOREA A., GELLERT A. – *Random Degrees of Unbiased Branches,* Proceedings of The Romanian Academy, Series A: Mathematics, Physics, Technical Sciences, Information Science, Volume 9, Number 3, pp. 259 - 268, ISSN 1454-9069, Bucharest, 2008 - http://www.academiaromana.ro/sectii2002/proceedings/doc2008-3/13-Vintan.pdf (**cotata ISI Thomson Journals** - http://scientific.thomsonreuters.com/cgi-bin/jrnlst/jlresults.cgi?PC=MASTER&ISSN=1454-9069); Impact Factor=0.333, cf. http://www.cncsis.ro/IC8/2009_files/Factor_relativ_ajustat.pdf
16. A. GELLERT, A. FLOREA, **L. VINTAN** - *Exploiting Selective Instruction Reuse and Value Prediction in a Superscalar Architecture*, Journal of Systems Architecture, vol. 55, issues 3, pp. 188-195, ISSN 1383-7621, Elsevier, 2009 (**cotata ISI Thomson Journals** - http://scientific.thomsonreuters.com/cgi-bin/jrnlst/jlresults.cgi?PC=MASTER&ISSN=1383-7621**,** http://dx.doi.org/10.1016/j.sysarc.2008.11.002, Impact Factor = 0.828 cf. http://www.cncsis.ro/IC8/2009_files/Factor_relativ_ajustat.pdf). Indexata in **ScienceDirect**, v. http://www.sciencedirect.com/science?

_ob=ArticleListURL&_method=list&_ArticleListID=902082850&_sort=d&view=c&_acct=C000064540&_version=1&_urlVersion=0&_userid=4714271&md5=2671eef6ddace41d9e490b73aaabb9f7

17. GELLERT A., PALERMO G., ZACCARIA V., FLOREA A., **VINTAN L.,** SILVANO C. - *Energy-Performance Design Space Exploration in SMT Architectures Exploiting Selective Load Value Predictions*, Design, Automation & Test in Europe International Conference (DATE 2010), March 8-12, 2010, Dresden, **Germany**, ISBN 978-3-9810801-6-2, pp. 271-274 (http://www.date-conference.com/front; 326 accepted papers from over 980 submitted papers! **DATE is the second prestigious conference in the world in EDA domain, after DAC**)

18. C. RADU, **L. VINTAN** - *Towards a Unified Framework for the Evaluation and Optimization of NoC Application Mapping Algorithms*, 6-th International HiPEAC Summer School on Advanced Computer Architecture and Compilation for High-Performance and Embedded Systems (ACACES), Terrassa (Barcelona), **Spain**, pp. 163-166, Published by FP7 HiPEAC Network of Excellence, ISBN 978 90 382 1631 7, July 2010 - http://www.hipeac.net/summerschool/index.php?page=home

19. H. CALBOREAN, **L. VINTAN** - *Toward an Efficient Automatic Design Space Exploration Frame for Multicore Optimization*, 6-th International HiPEAC Summer School on Advanced Computer Architecture and Compilation for High-Performance and Embedded Systems (ACACES), Terrassa (Barcelona), **Spain**, pp. 135-138, Published by FP7 HiPEAC Network of Excellence, ISBN 978 90 382 1631 7, July 2010 - http://www.hipeac.net/summerschool/index.php?page=home

Evaluation Modalities

Examination form: writing
The final mark (FM) will include:

a) homeworks (N1) – 20%
b) applications' activity (N2) – 30%
c) final exam (N3) – 50%

FM=0,2×N1+0,3×N2+0,5×N3
Eligibility Condition: minimum 5 mark for each component (N1, N2, N3).

Curricula's Updating & Improving Modalities

Based on the most prestigious international text-books and also based on the most relevant progresses in this field (as these developments are presented in top-level scientifical reviews, research projects and international conferences). This updating process is facilitate due to the fact that Professor Vintan is a Visting Research Fellow at Herfordshire University – see http://homepages.feis.herts.ac.uk/%7Ectca/, collaborator of Department of Computer Science from Augsburg University (prof. Theo Ungerer), European Commission DG Information Society Expert European FP6/FP7 NoE "High Performance Embedded Architectures and Compilers" – HiPEAC, see www.hipeac.net, Siemens CT IC Munich Counsellor**,** Member of many International Program Committees Conferences and Scientific Reviewer to IEE Proceedings - Computer and Digital Techniques, United Kingdom, etc.

E. Correlations with other topics belonging to the Curricula

Based on periodic (each semester) teaching plan & curricula analysis involving all colleagues activating in this Master program.

Metode de predare / seminarizare	Expunerea (clasica -deductiva, inductiva si formalizata; expuneri PPT etc.), conversaţia euristică, problematizare, studii de caz, prelegere intensificată, teme de casa. Se utilizeaza inclusiv si predilect, vechile principii ale educatiei paideice, in virtutea carora, studenti si lector deopotriva, dau si primesc cunostinte.

Stabilirea notei finale (procentaje)	- răspunsurile la examen/colocviu(evaluare finală)	50%
	- teste pe parcursul semestrului	20%
	- răspunsurile finale la lucrările practice de laborator	30%
	- activitaţi gen teme/referate/eseuri/traduceri/proiecte etc.	
	- teme de control	10%
	- alte activităti*(precizaţi)*…… ……..	
	- TOTAL	100%

Descrieţi modalitatea practică de evaluare finală, E/V (de exemplu: lucrare scrisă (descriptive şi/sau test grilă şi/sau probleme etc.), examinare orală cu bilete, colocviu individual ori în grup, proiect etc)

Evaluarea finală va cuprinde rezolvarea a 5-6 probleme cu un pronuntat caracter aplicativ (asigurand inclusiv verificarea stapanirii conceptelor teoretice esentiale), fiecare cuprinzand 2-4 sub-probleme. Subiectele vor acoperi intreaga problematica cuprinsa in programa analitica. Aceste probleme totalizeaza 100 de puncte, repartizate judicios, functie de dificultatea specifica a fiecarei sub-probleme.

Cerinţe minime pentru nota 5	**Cerinţe pentru nota 10**
• Nota 5 la activităţi aplicative la laborator, temelor si testelor pe parcurs; • Nota 5 la examenul propriu-zis (adica minim 50 puncte din cele 100 puncte aferente problemelor examenului final)	- punctaj maxim pentru toate activitatile din timpul semestrului; - peste 95 puncte la examenul final. Pentru rezutate deosebite în activitatea de cercetare se acordă bonificaţii de până la 2 puncte la nota finală (conform regulamentului de evaluare al Facultăţii de inginerie).
TOTAL ore studiu individual (pe semestru) = 70	

Bibliografia	**Minimală obligatorie**: . • **VINTAN N. LUCIAN** – *Prediction Techniques in Advanced Computing Architectures* (in English Language), Matrix Rom Publishing House, Bucharest, 2007 (292 pg.); comenzi la **www.matrixrom.ro** • **VINTAN N. LUCIAN** – *Documentatii (articole, prezentari PPT, teze etc.) aferente acestei discipline,* URL: **http://webspace.ulbsibiu.ro/lucian.vintan/index.html#11** . **Complementară:** **1. VINTAN N. LUCIAN –** *Arhitecturi de procesoare cu paralelism la nivelul instructiunilor*, Editura Academiei Romane, Bucuresti, 2000 (264 pg.), ISBN 973-27-0734-8 – comanda la **www.ear.ro**, Bibl. ULBS, cota 45.351 (15 ex. la Biblioteca ULBS) **2. VINTAN LUCIAN, FLOREA ADRIAN** - *Sisteme cu microprocesoare - aplicatii*, Editura Universitatii "L. Blaga" din Sibiu, ISBN 973-9410-46-4 , Sibiu, 1999 (245 pg.) Bibl. Univ. Sibiu, cota 43.800 (15 ex. intern + 15 ex. schimb interbibliotecar) **3. VINTAN N. LUCIAN, FLOREA ADRIAN** – *Microarhitecturi de procesare a informatiei*, Editura Tehnica, Bucuresti, ISBN 973-31-1551-7, cota bibl. ULBS 45.797 (16 schimb+14 intern bibl.ULBS), 2000 (312 pg) **4. FLOREA ADRIAN, VINTAN N. LUCIAN** – *Simularea si optimizarea arhitecturilor de calcul in aplicatii practice*, Editura Matrix Rom, Bucuresti, ISBN 973-685-605-4, 2003 (443 pg. + CD atasat), Bibl. Univ. Sibiu - cota 48.351 (4 ex. la Biblioteca ULBS + 4 ex. schimb interbibliotecar); comenzi la **www.matrixrom.ro** **5. VINTAN LUCIAN**.- *Generaţia următoare,* în revista PC-Report, nr.3, Editura Computer Press Agora, ISSN 1220-9856, martie, 2000 **6.VINTAN LUCIAN**.- *Procesorul IA-64: între evoluţie şi revoluţie,* în revista PC-Report, nr.5, Editura Computer Press Agora, ISSN 1220-9856, mai, 2000 **7.VINTAN LUCIAN**.- *Organizarea si proiectarea microarhitecturilor. Note de curs* (pdf, 270 pagini A4), URL: **http://webspace.ulbsibiu.ro/lucian.vintan** **7. HENNESSY J., PATTERSON D.** - *Computer Architecture: A Quantitative Approach*, Morgan Kaufmann (Elsevier), 3rd Edition, 2003 **8. PATTERSON D., HENNESSY J**. - *Computer Organization and Design, The Hardware/ Software Interface*, Morgan Kaufmann Publishers, 2nd Edition, 1998 (traducere romaneasca la Editura ALL, Bucuresti, 2000) **9. FISHER J., FARABOSCHI P., YOUNG C. –** *Embedded Computing***,** Morgan Kaufmann Publishers (Elsevier), 2005 **10. HAYES J.** – *Computer Architecture and Organization*, Third Edition, McGraw Hill, 1998 **11. JERRAYA A., WOLF W. (Editors)** – *Multiprocessors Systems on Chips*, Morgan Kaufmann Publishers (Elsevier), 2005

Lista materialelor didactice utilizate în procesul de predare:

Tabla şi creta; videoproiector si laptop, prezentari PPT ale cursului; curs si indrumar de aplicatii, publicate, existente la Biblioteca ULBS dar si in format electronic pe pagina de web a titularului de curs - **http://webspace.ulbsibiu.ro/lucian.vintan/**.

Retea de calculatoare, Sisteme operare: Linux, Windows, Instrumente soft: Visual C++ v.6.0, set utilitare GCC, set simulatoare SimpleScalar v.3.0 si M-SIM (SMT), simulatoare LC-2, SPIM, DLX, SATSim, set simulatoare complexe pentru optimizarea microarhitecturilor avansate (dezvoltate local), simulator CACTI si Watch (consum putere), benchmark-uri SPEC 2000, benchmark-uri Stanford-HSA. Frame-urile de cercetare dezvoltare UniSim, Multi2Sim, Msim, M5 etc. pentru arhitecturi multi si *many-cores*.

	Grad didactic, titlul, prenume, numele	Semnătura
Coordonator de disciplină	**Prof.univ.dr.ing. Lucian VINTAN Membru (c.) al Acad. de Stiinte Tehnice din Romania**	

22.09.2010

ŞEF CATEDRĂ

Conf. dr. ing. Ioan Z. MIHU